

# FIRST DEMONSTRATION OF A 0.5 W, 2 TO 8 GHZ MMIC HBT DISTRIBUTED POWER AMPLIFIER BASED ON A LARGE SIGNAL DESIGN APPROACH

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## ABSTRACT

*In this paper we report the results of the first demonstration of a 0.5 Watt, 2 to 8 Ghz MMIC HBT distributed power amplifier optimised with a new design methodology. Initially developed for MESFET transistors, this new design methodology has been applied to HBT devices to obtain simultaneously both high power and high efficiency operation. Thus, a power density performance greater than 1W/mm has been demonstrated, compared to the MESFET where a typical value of 0.35W/mm can be observed. Moreover, an average value of 20 % power added efficiency between 2 and 8 GHZ has been measured with a peak efficiency of 30 % at 3 Ghz.*

## I- INTRODUCTION

Electronic warfare applications or phase array radar require wide and narrow band MMIC amplifier where both power and high efficiency are desired simultaneously. Although lots of improvements have been made on the MESFET, they do not allow to develop power MMIC with high efficiency, especially for wide band amplifiers where 15 % seems to be the maximum achievable value. At the opposite, heterojunction bipolar transistor (HBT) have already demonstrated very high power added efficiency for both wide and narrow band applications [1], [2]. Consequently HBT is now considered as one of the best component to design highly efficient MMIC power amplifier. While both power and efficiency are determined by the active devices used in the MMIC, the bandwidth depends essentially on the topology of the amplifier. Distributed amplifier is the best solution to develop very wide band amplifier, but leads to small power density performance associated with low efficiency when classical design technique is used. Nevertheless, in [3] a new design methodology based on a large signal approach is proposed for MESFET to optimise the output power provided by all the active devices. Thus, the aim of this article is to demonstrate

that this new method can be applied to HBT to develop a high efficiency wide band power amplifier.

To illustrate the proposed methodology, we describe the circuit design and the first run of a 0.5 Watt, 2 to 8 Ghz MMIC HBT distributed power amplifier optimised for power with 8 dB small signal gain and an average value of 20 % power added efficiency. To our knowledge, this is the first reported distributed amplifier optimised in power using HBT.

## II- CIRCUIT DESIGN METHOD

Distributed amplifier represents the typical circuit solution when very wide band (more than two octaves) performance is required. The conventional design technique of power distributed amplifiers is to optimise the circuit for small signal gain using the largest possible transistor that will simultaneously provide the required output power with the desired gain at the highest frequency. Therefore this conventional distributed design technique results in a small power density and efficiency, because each active device delivers only a small part of their available output power. Nevertheless, optimum power performance can be obtained in a distributed amplifier by taking into account with special care large signal requirements. In short, the design methodology to develop MESFET optimum power distributed amplifier is based on a power load requirement and the equalisation of the control voltage. To equalise the control voltage, the classical structure of a distributed amplifier has been modified by adding series capacitors between the active devices and the gate line (figure N°1). These ones allow to achieve a larger input power as well as equal drive level on the gate. Moreover, the drain line must be designed to match as closely as possible the optimum power load over the frequency range for each active device used in the MMIC.

To apply these non-linear design methodology to the HBT, some differences between HBT and MESFET devices must be taken into account. Indeed, with HBT devices, the most critical point to develop a distributed

amplifier optimised for power is the input impedance. In particular the base-emitter capacitance in HBT devices ( $C_{be}$ ) is near 10 times greater than the gate-source capacitance in the MESFET ( $C_{gs}$ ) for the same output power capability. Consequently, due to the value of  $C_{be}$  it is very difficult to synthesize the input transmission line of the distributed amplifier over the frequency range. The solution was to use the added series capacitors between the devices and the input transmission line, to reduce the equivalent input capacitance of the HBT device. In this case it was easier to synthesize the input transmission line over the frequency range. Thus, special care must be taken in the optimisation process to reach the best trade-offs between optimum power load, amplifier gain, and input return loss. These design concepts result in a gain reduction but provide better gain compression characteristics for power operation. One of the key points to design a distributed power amplifier is to use an accurate HBT non-linear model and the optimum power load.

### III- LARGE SIGNAL MODEL

Typically, for wide band applications the model used for the design is optimised, at least, to reproduce S parameters over the required frequency range. Nevertheless, to design an optimum distributed power amplifier the model should also reproduce the large signal behaviour of the active device to match accurately the optimum power load presented at each device. Moreover, the model should recognise the fact that the DC and the Rf responses may be different due to the parasitic effects. In particular, within HBT devices, thermal effects are very important. Thus, for the modelling work we performed a comprehensive set of measurements on several discrete HBTs devices with a pulsed measurement system to ensure that the device is maintained at a constant temperature during the characterisation process [4].

For the MMIC design we used a typical HBT large signal model (figure 2) where all the non-linearities have been determined with pulsed I(V) and broad band (up to 20 GHz) S parameters measurements performed at multiple bias points in the whole operating regions of the device including low collector currents, breakdown and knee region. To take into account the temperature effects, the pulsed characterisation has been performed around a quiescent bias point chosen to represent the thermal rise of the HBT when operating within the amplifier. For this, we considered that the amplifier will operate in class A and that the power added efficiency will be near 20 %. Then, with the well known expression given in (1), we evaluated the dissipated power within the transistor

during the amplifier operation and so the quiescent bias point. Moreover, the methodology used to determine the value of each element of the large signal model is based on a direct extraction process which has been previously published in [5].

$$(1) P_d = P_o (1 - RPA)$$

### IV- MMIC REALISATION AND TEST RESULTS

A 2 to 8 GHz HBT distributed power amplifier operating in class A has been designed using the methodology previously described. The MMIC has been manufactured at THOMSON Central Research Laborator (LCR) in FRANCE and it provided a minimum output power of 500 mW over the frequency range with an average power added efficiency of 20 %. A photograph of the circuit is given figure 3. The unit cell used for the MMIC design is a 0.3W common emitter GaInP/GaAs HBT. This unit cell has four  $2 \times 30 \mu\text{m}^2$  emitter fingers arranged in two rows and two columns [6]. The small signal gain of this device is about 11 dB at 10 GHz and the typical output optimum power load can be approximated at  $14\text{mS} // 0.32\text{pF}$  over the required frequency range.

During the optimisation procedure we searched to reach the best trade-offs between the amplifier gain, the input return loss and the optimum power load by synthesising simultaneously the input and the output transmission lines. On figures 4a et 4b we present the variation of both real and imaginary part of the admittance synthesised at the output of each transistor obtained after the optimisation procedure. We can see that it is very difficult to match precisely all the devices over the required frequency band and in particular, we note that the first transistor (T1) is not accurately matched, but it is classical for an optimum power distributed amplifier [3]. Nevertheless the others devices (T2 to T4) are correctly matched and they are able to deliver their maximum output power. Moreover, base emitter bias is applied through a resistor placed between the transistor and the input transmission line in parallel with the added input capacitor, chosen to reach the best trade-offs between the small signal gain and the efficiency. In our case, the optimum value was 400 Ohms. Thus, on figure 5 we present the simulated and measured small signal gain and input return loss. On figure 6 we present the results of the large signal simulations and measurements of the HBT distributed power amplifier at 6 GHz.

Several power measurements have been performed on this HBT MMIC distributed power amplifier. Some amplifiers were mounted in a test fixture

## V- CONCLUSION

## ACKNOWLEDGEMENT

## REFERENCES

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- [5] - **J.P. Viaud and al** "*Non linear Rf characterisation and modelling of heterojonction bipolar transistors under pulsed conditions*", 24th EuMc, pp1610-1615, Cannes 1994.
- [6] - **S. L. Delage and al** "*Power GaInP/GaAs HBT MMICs*" 24EuMc, pp1143-1148, Cannes 1994.

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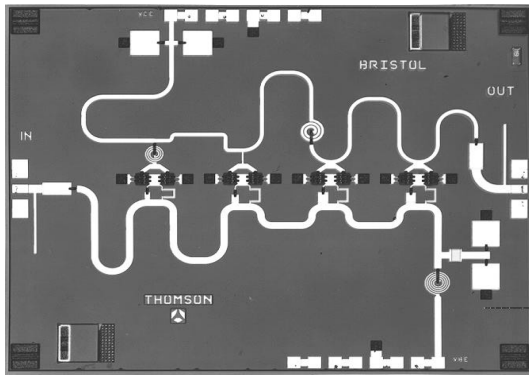


Figure N°3 : Photograph of the 2 to 8 GHz HBT MMIC amplifier. The chip size is  $3.8 \times 3 \text{ mm}^2$

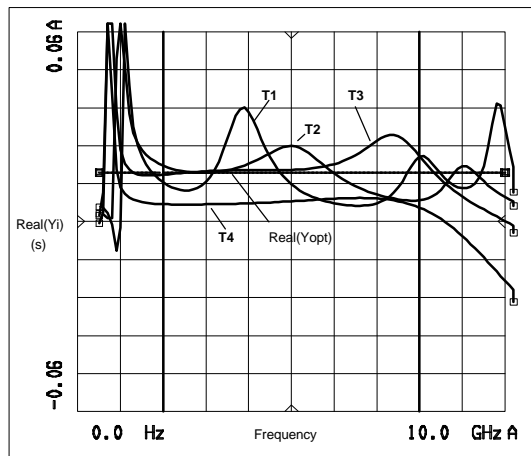


Figure 4a : Real part of the admittance presented on the output of each devices compared to the real part of the optimum power load

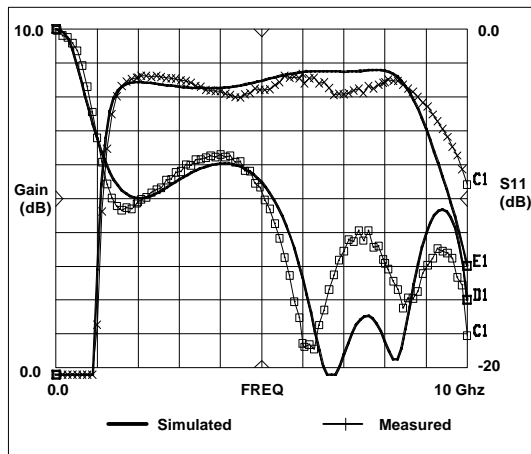


Figure 5 : Comparison between Measured and simulated small signal data

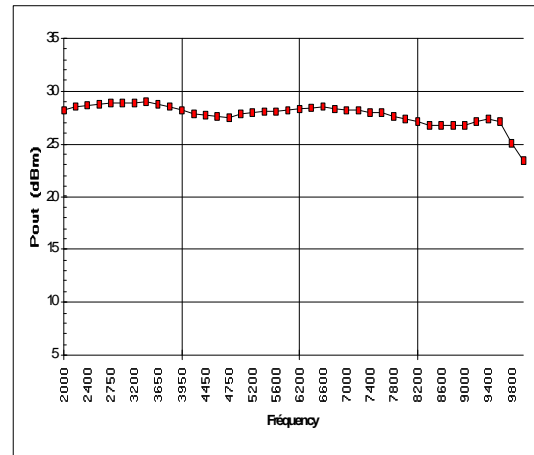


Figure 7 : output power measured with an input power of 22 dBm and a collector voltage of 8Volts

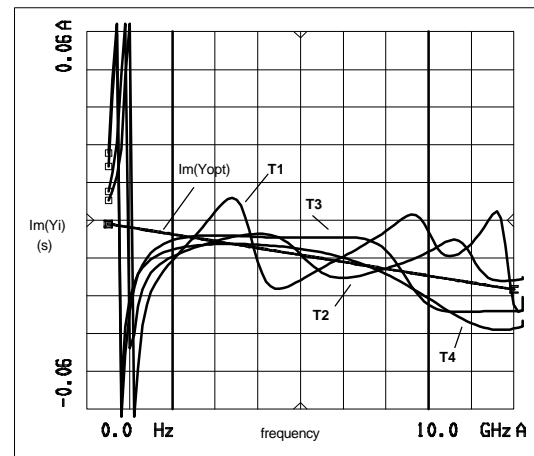


Figure 4b : Imaginary part of the admittance presented on the output of each devices compared to the imaginary part of the optimum power load

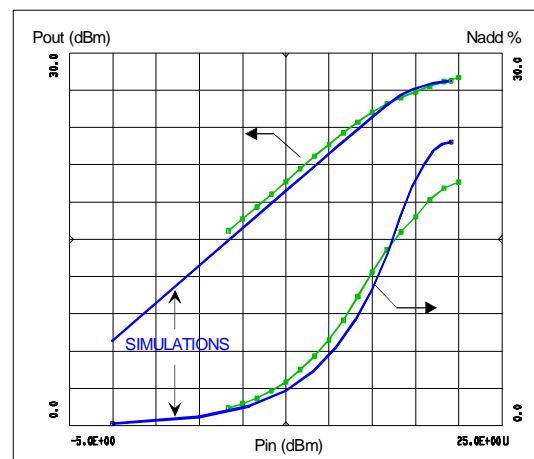


Figure 6 : Measured and simulated large signal performances obtained at 6 GHz without circuit tuning

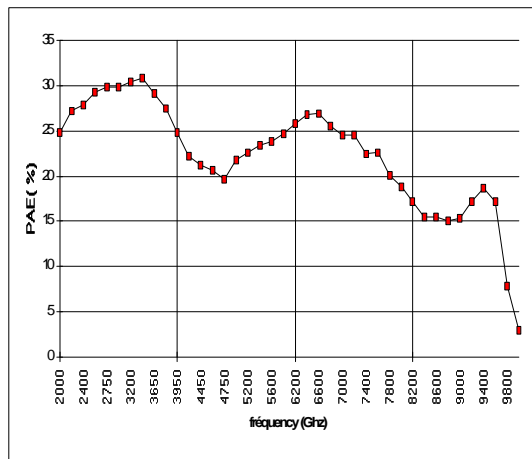


Figure 8 : PAE measured with an input power of 22 dBm and a collector voltage of 8 volts